M.Sc. Sem III

MPHYCC - 12

electronics II

OP-amp

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Individual Sequential Logic circuits can be used to build more Complex circuits such as Multivibrators, Counters, Shift Registers Latches & Memories.

But for These types of Circuits to operate in a sequential way They require The addition of some form of clock Pulse or timing Signal to Cause Them to change Their State. clock Pulses are generally continuous Square or rectangular Shaped waveform which are produced by a single Pulse generator circuit such as a Multivibrator.

A multivibrator circuit oscillates between a "High" state and a "Low" state producing a Continuous output.

There are basically Three types of clock Pulse generation Circuits.

1.) Astable :- A free-running multivibrator that has no stable states but switches continuously between two states This action produces a train of Square wave Pulses at a fixed Known frequency

2.) Monostable - A one-shot multivibrator That has only ONE Stable State as once externally triggered it returns back to its first stable state.

3.) Bistable — A flip-flop That has Two stable states producing a single Pulse either HIGH or LOW in Value.

one way of producing a very simple clock signal is by the interconnection of digital logic gates. As NAND gates contain current amplification, they can also be used to provide a suitable clock signal or timing pulse with the aid of a single capacitor and resistor to provide the required feedback and timing functions.

These timing circuits are often used because of there simplicity and are also useful if a logic circuit once designed has some unused gates which can be utilised to create a monostable or astable oscillator. This simple type of RC oscillator network is sometimes called a Relaxation Oscillator".

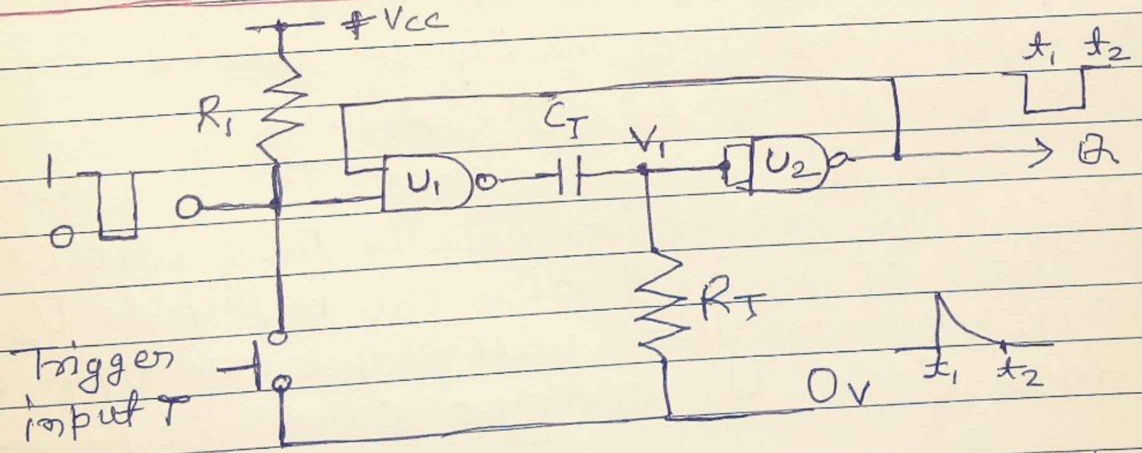
Monostable Multivibrator Circuits :-

Monostable multivibrators or "one shot" pulse generators are generally used to convert short sharp pulses into much wider ones for timing applications. Monostable multivibrators generate a single output pulse, either "HIGH" or "LOW", when a suitable external trigger signal or start pulse T is applied.

This trigger pulse signal initiates a timing cycle which causes the output of the monostable to change state at the start of the timing cycle (t_1). The output remains in this second state until the end of the timing period. (t_2) which is determined by the time constant of the timing capacitor C_T and the resistor. R_T.

The monostable multivibrator now stays in this second timing state until the end of the RC time constant and automatically "resets" or returns itself back to its original (stable) state. Then a monostable circuits has only one stable state which is its idle or rest state. A more common name for this type of circuit is simply a "Flip Flop" as it can be made from two cross-coupled NAND gates (or NOR gates) as we have seen previously consider the circuit below

Simple NAND gate Monostable Circuit :-



Suppose that initially the trigger input T is held HIGH at logic level '1' by the resistor R_1 so that the output from the first NAND gate U_1 is LOW at logic level "0". The timing resistor R_T is connected to a voltage level equal to logic level "0". Which will cause the capacitor, C_T to be fully discharged. The output of U_1 is therefore LOW. As the timing capacitor is completely discharged, junction V_1 will also be equal to "0" resulting in the output from the 2nd NAND gate U_2, which is connected as an inverting NOT gate to be HIGH (logic 1)

The output from the 2nd NAND gate (U_2) is fed back to one input of U_1 to provide the necessary +ve feed back. Since the junction V_1 and the O/T of U_1 are both at logic "0" no current flows in the timing capacitor C_T. This result in the circuit being stable and it will remain in this stable state until a trigger input T is applied.

If a -ve pulse is now applied either externally or by the action of the push-button to the trigger input of the NAND gate U_1, the O/T of U_1 will go HIGH to logic "1".

Since the voltage across the capacitor cannot change instantaneously this will cause the junction at V_1 and also the input to U_2 to go HIGH, which in turn will make the O/T of the NAND gate U_2 change state to logic 0.

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The Circuit will now remain in This 2nd timing state even if The trigger input Pulse T is removed. This is Known as The Meta - stable state.

The Voltage across The capacitor will now increase as The capacitor C_T starts to charge up from The HIGH output of U_1 at a time constant deter- mined by The resistor / capacitor combination. This Charging Process Continues until The charging current is unable to hold The input of U_2 and Therefore junction V_1 HIGH.

when This happens, The output of U_2 switches HIGH again, logic-1 which in turn causes the output of U_1 to go LOW and The capacitor discharges into The output of U_1 under the in- fluence of resistor R_T. The Circuit has now switched back to its original stable state.

Thus for each -ve going trigger pulse, The monostable Multivibrator Circuit produces a LOW going output Pulse. The length of The output time Period is determined by The capacitor/resistor Combination and is given as The Time constant $T = 0.69RC$ of The Circuit in seconds. Since The input impedance of The NAND gates is very high, large timing Periods can be achieved.

As well as the NAND gate monostable type circuit above, it is also Possible to

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build simple monostable timing circuits that start their timing sequence from the rising-edge of the trigger pulse using NOT gates, NAND gates and NOR gates connected as inverters as shown below —